Chettinad
College of Engineering & Technology
Approved by AICTE-New Delhi and Affiliated to Anna University-Chennai

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CEC354 ANALOG ICDESIGN

ACADEMIC YEAR: 2023-2024

III YEAR/VI TH Semester Lab Manual

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CEC334 ANALOG IC DESIGN

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OBJECTIVES:

The student should be made to:

- To study the basics of MOS Circuits.
- To analyse the noise characteristics of amplifiers.
- To study the performance parameters of amplifiers.
- To comprehend the compensation techniques
- To understand the detection and testing of faults.

LIST OF EXPERIMENTS:

1. Design a CMOS inverter and analyze its characteristics.
2. Design a Common source amplifier and analyze its performance.
3. Design a Common drain amplifier and analyze its performance.
4. Design a Common gate amplifier and analyze its performance.
5. Design a differential amplifier with resistive load using transistors.
6. Design three stage and five stage ring oscillator circuit and compare its frequencies.

List of equipment needed for a batch of 30 students (3 in a bench):

- Cadence/Tanner/equivalent EDA Tools -10 User

TOTAL: 30 PERIODS

COURSE OUTCOMES:

At the end of the course, the student should be able to

CO1: Design amplifiers to meet user specifications.

CO2: Analyse the frequency and noise performance of amplifiers.

CO3: Design and analyse feedback amplifiers and one stage op amps .

CO4: Analyse stability of op amp.

CO5: Testing experience of logic circuits.

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S.No	Name of the Experiment	Page No	Marks Obtained	Signature of the faculty member.
1	Design a CMOS inverter and analyze its characteristics.			
2	Design a Common source amplifier and analyze its performance.			
3	Design a Common drain amplifier and analyze its performance			
4	Design a Common gate amplifier and analyze its performance.			
5	Design a differential amplifier with resistive load using transistors.			
6	Design three stage and five stage ring oscillator circuit and compare its frequencies.			

EX.NO.1 Design a CMOS inverter and analyze its characteristics.

AIM :

To design, synthesize, simulate and implement the CMOS inverter in layout form using Microwind.

APPARATUS REQUIRED :

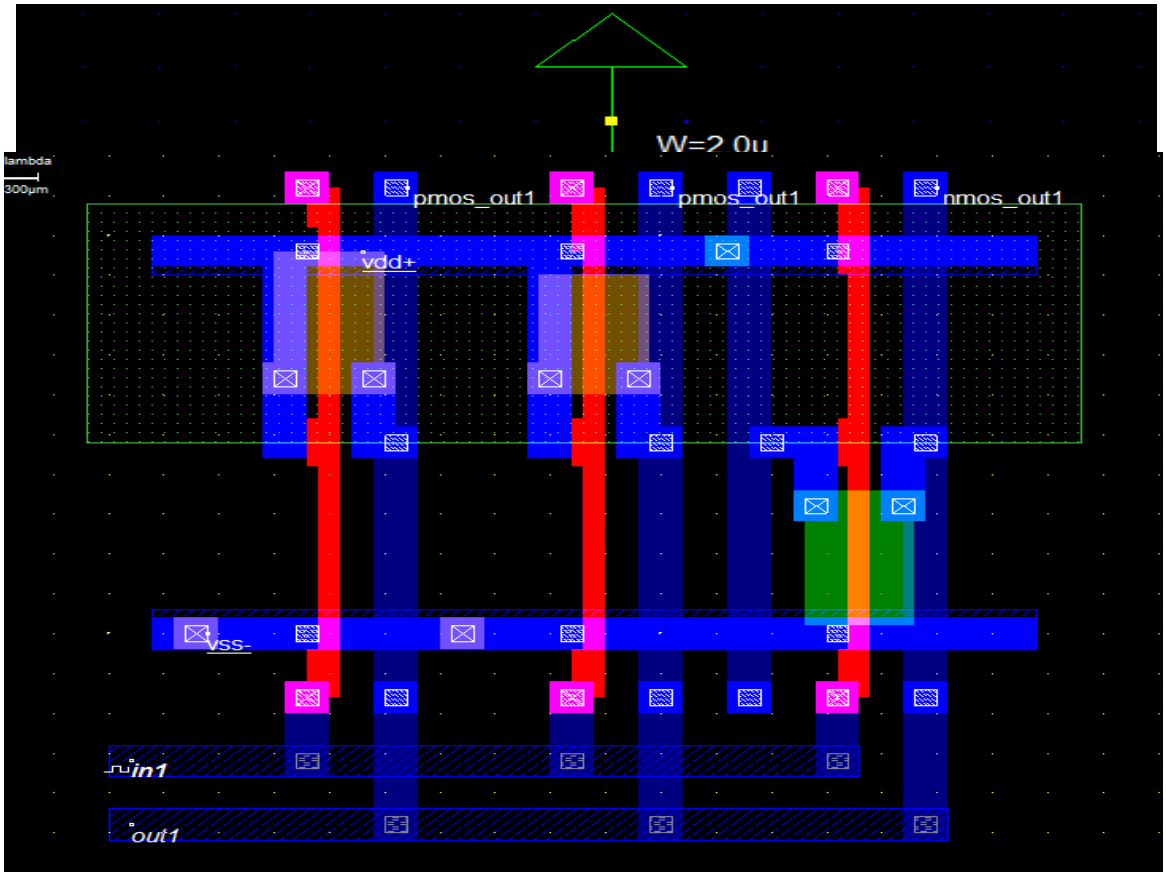
*PC

*microwind

THEORY:

CMOS inverter consists of a series connection of a PMOS and an NMOS. VDD represents the voltage of logic 1, while the ground represents logic 0. Whenever the input is high or 1, the NMOS is switched on while the PMOS is turned off. Thus output Y is directly connected to the ground and thus comes to be logic 0

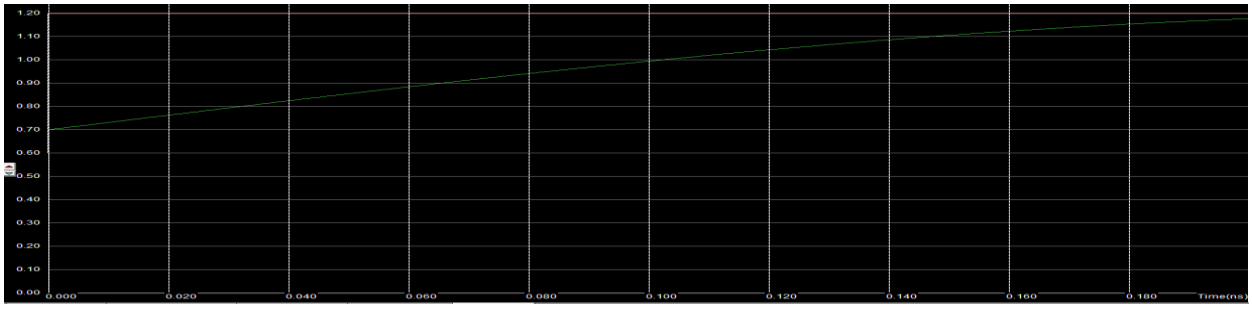
CMOS INVERTER

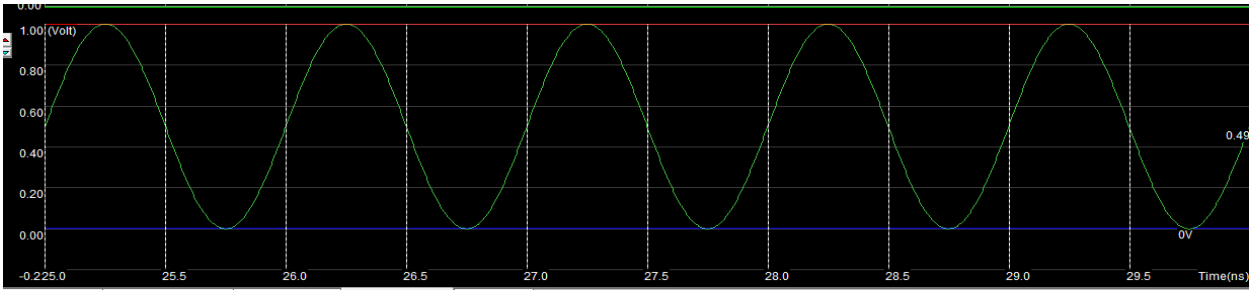


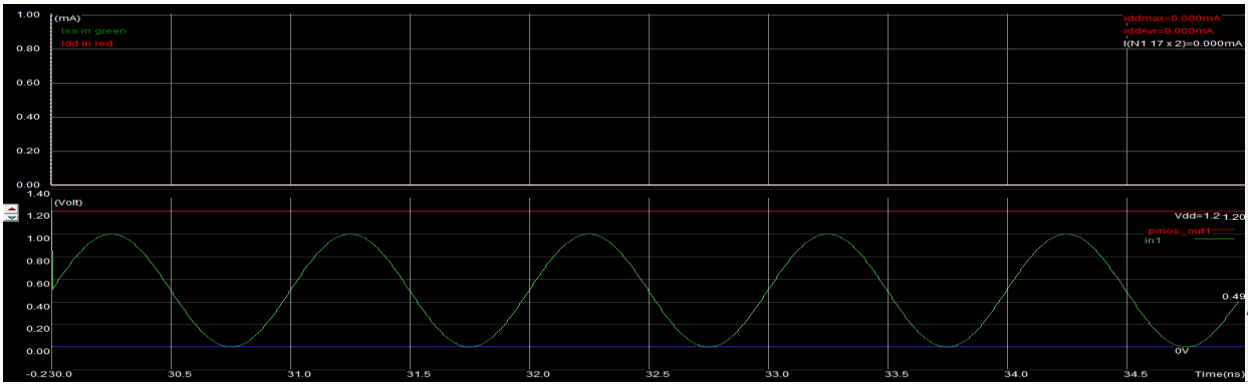
WAVE FORM

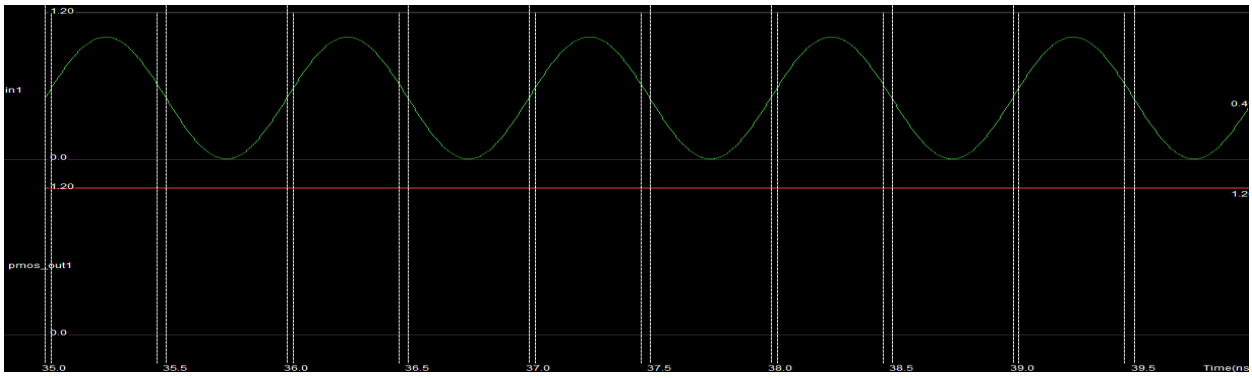
(NOTE:Double click in1=> click sinus

set =>AMP =0.1,OFFSET=0.7)









NETLIST

```
CIRCUIT example
*
IC Technology: CMOS 0.12µm - 6 Metal
*
VDD 1 0 DC 1.20
*
List of nodes
" nmos_out3" corresponds to n°3
"N4" corresponds to n°4
"in4" corresponds to n°5
*
MOS devices
MN1 3 5 1 0 N1  W= 0.90U L= 0.12U
MN2 4 3 3 0 N1  W= 1.02U L= 0.12U
*
C2 1 0  2.578fF
C3 3 0  1.502fF
C4 4 0  0.497fF
C5 5 0  0.365fF
   *
n-MOS Model 3 :
low leakage
.MODEL N1 NMOS LEVEL=3 VTO=0.40 UO=600.000 TOX= 2.0E-9
+LD =0.000U THETA=0.500 GAMMA=0.400
+PHI=0.200 KAPPA=0.060 VMAX=120.00K
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p CJSW=240.0p
*
Transient analysis
*
.TEMP 27.0
.TRAN 0.1N 5.00N
(Pspice)
.PROBE
.END
```

PROCEDURE:

1.Open microwind by double clicking on microwind.
2.Create new design by click on file-new
3.Select model file by click on file->select foundary and select the model file and save the file4.Make Verilog file and click on generate
5.To run the simulation file
6.View the output waveform

PARTICULARS	MAXIMUM MARKS	MARKS OBTAINED
PREPARATION	30	
EXECUTION OF PRACTICAL	30	
CONCLUDING ACTIVITIES	30	
VIVA-VOCE	10	
TOTAL MARKS	100	

RESULT:
Thus the CMOS inverter schematic form was designed and simulated using Microwind.

EX.NO. 2 DESIGN AND SIMULATE COMMON SOURCE

GENERATE LAYOUT

AIM :

To design, synthesize, simulate and implement the Common source in layout form usingMicrowind.

APPARATUS REQUIRED :

*PC

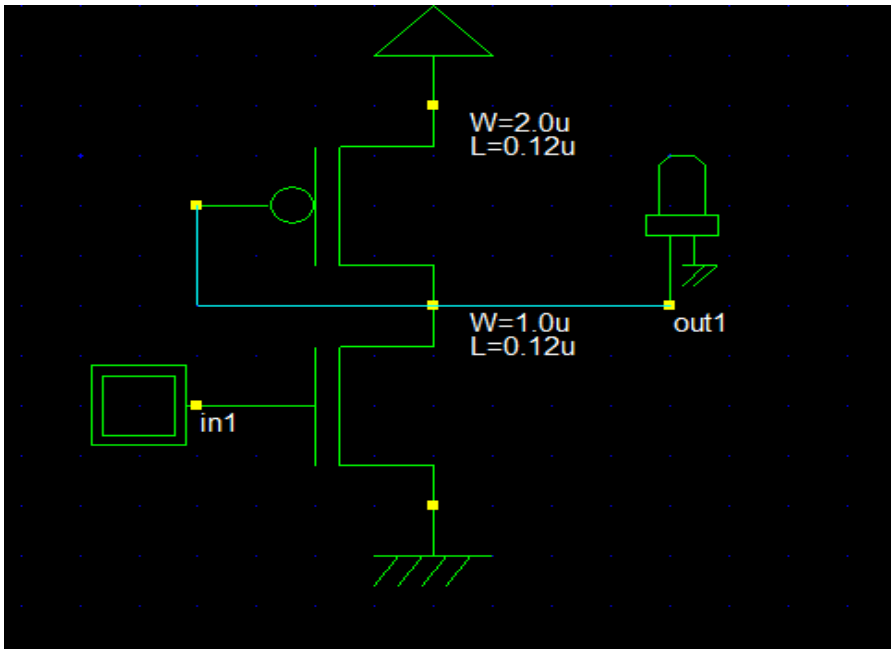
*microwind

THEORY:

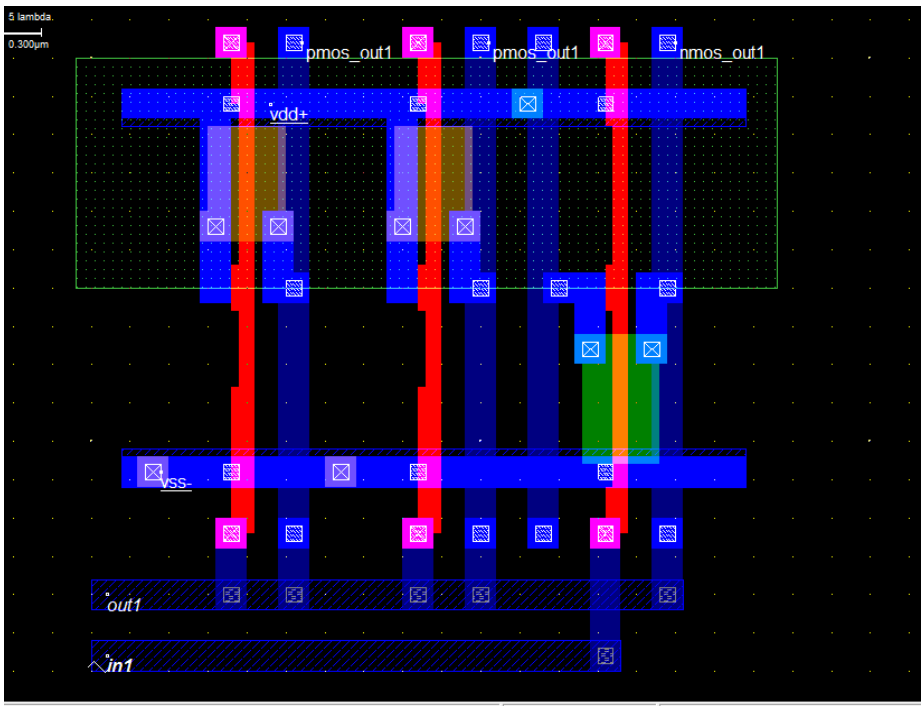
In electronics, a **common-source** amplifier is one of three basic single-stage field-effect transistor (FET) amplifier topologies, typically used as a voltage or transconductance amplifier. The easiest way to tell if a FETis common source, common drain, orcommon gate is to examine where the signal enters and leaves. The remaining terminal is what is known as "common". In this example, the signal enters the gate, and exits the drain. The only terminal remaining is the source. This is a common-source FET circuit. The analogous bipolarjunction transistor circuit is the common-emitter amplifier.

COMMON SOURCE AMPLIFIER:

BLOCK DIAGRAM:



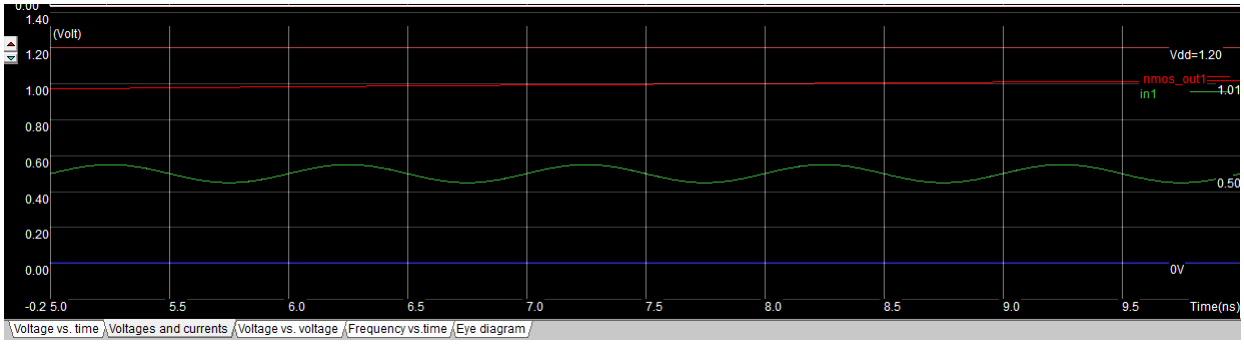
MICROWIND LAYOUT

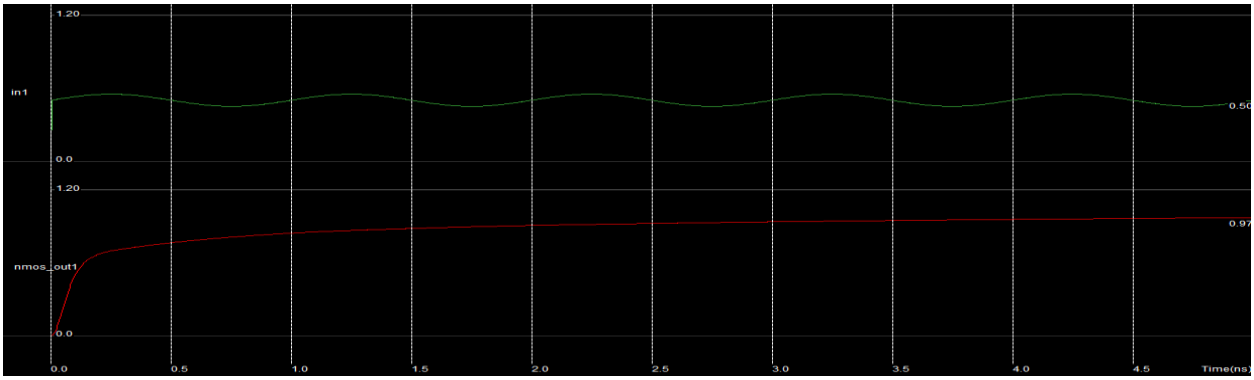


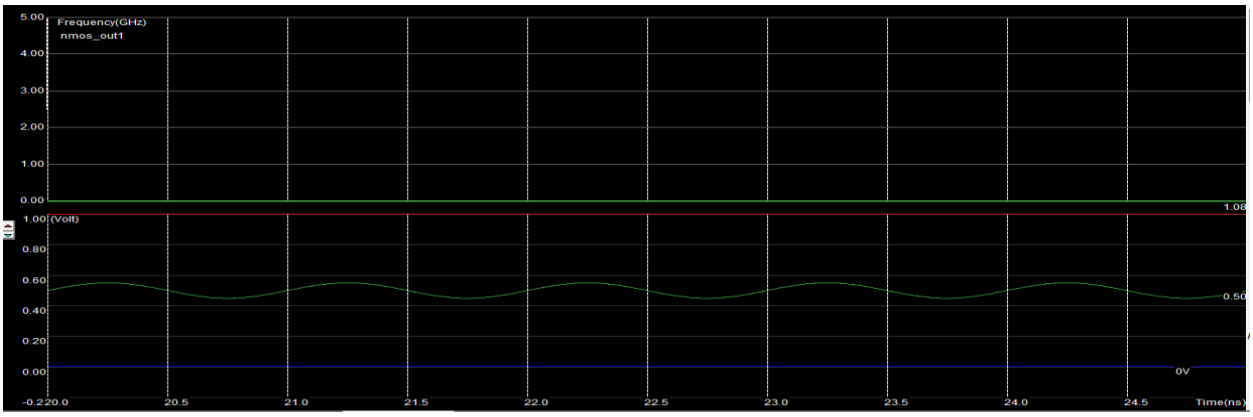
WAVE FORM

(NOTE:Double click in1=> click sinus

set =>AMP =0.05,OFFSET=0.5)







NET LIST

```
CIRCUIT example
*
* IC Technology: CMOS 0.12µm - 6 Metal
*
VDD 1 0 DC 1.20
*
 * List of nodes
 * " nmos_out1" corresponds to n°3
 * "N5" corresponds to n°5
 * "in1" corresponds to n°6
*
 * MOS devices
MN1 5 6 3 0 N1  W= 1.02U L= 0.12U
MP1 1 3 3 1 P1  W= 1.80U L= 0.12U
*
C2 1 0  3.555fF
C3 3 0  2.291fF
C5 5 0  0.497fF
C6 6 0  0.494fF
*
 * n-MOS Model 3 :
 * low leakage
.MODEL N1 NMOS LEVEL=3 VTO=0.40 UO=600.000 TOX= 2.0E-9
+LD =0.000U THETA=0.500 GAMMA=0.400
+PHI=0.200 KAPPA=0.060 VMAX=120.00K
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p CJSW=240.0p
*
 * p-MOS Model 3:
 * low leakage
.MODEL P1 PMOS LEVEL=3 VTO=-0.45 UO=200.000 TOX= 2.0E-9
+LD =0.000U THETA=0.300 GAMMA=0.400
+PHI=0.200 KAPPA=0.060 VMAX=110.00K
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p CJSW=240.0p
*
 * Transient analysis
*
.TEMP 27.0
.TRAN 0.1N 5.00N
 * (Pspice)
.PROBE
.END
```

PROCEDURE:

1.Open microwind by double clicking on microwind.
2.Create new design by click on file-new
3.Select model file by click on file->select foundary and select the model file and save the file
4.Make Verilog file and click on generate
5.To run the simulation file
6.View the output waveform

PARTICULARS	MAXIMUM MARKS	MARKS OBTAINED
PREPARATION	30	
EXECUTION OF PRACTICAL	30	
CONCLUDING ACTIVITIES	30	
VIVA-VOCE	10	
TOTAL MARKS	100	

RESULT:

Thus the common source schematic form was designed and simulated using microwind

EX.NO. 3 DESIGN AND SIMULATE COMMON DRAIN

GENERATE LAYOUT

AIM :

To design, synthesize, simulate and implement the CMOS drain in layout form usingMicrowind.

APPARATUS REQUIRED :

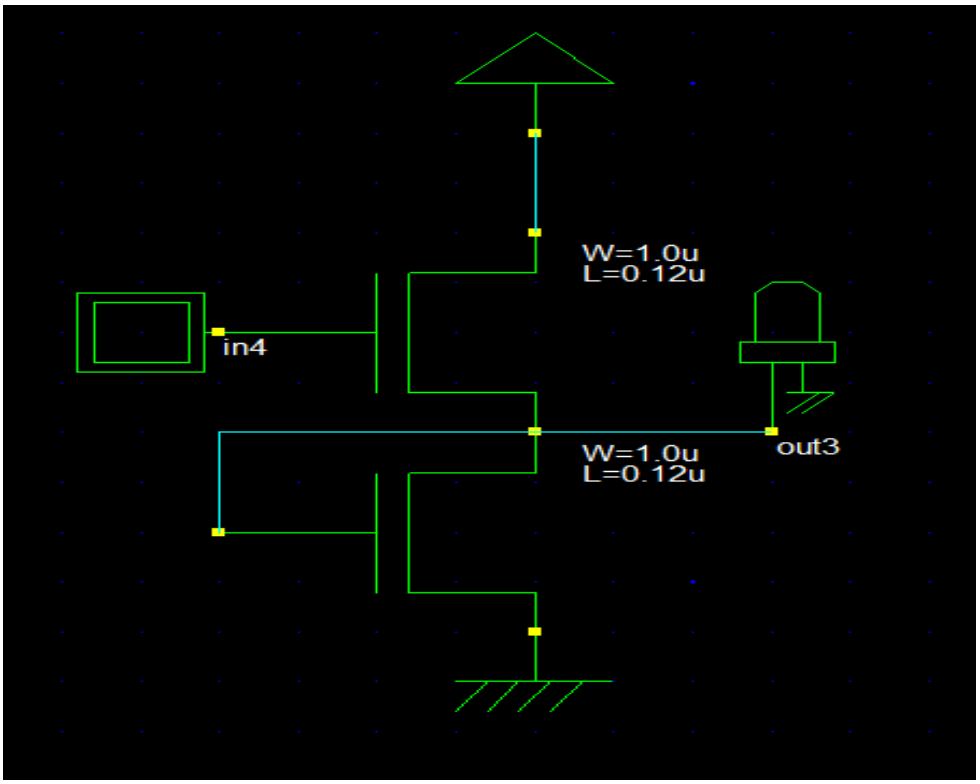
*PC

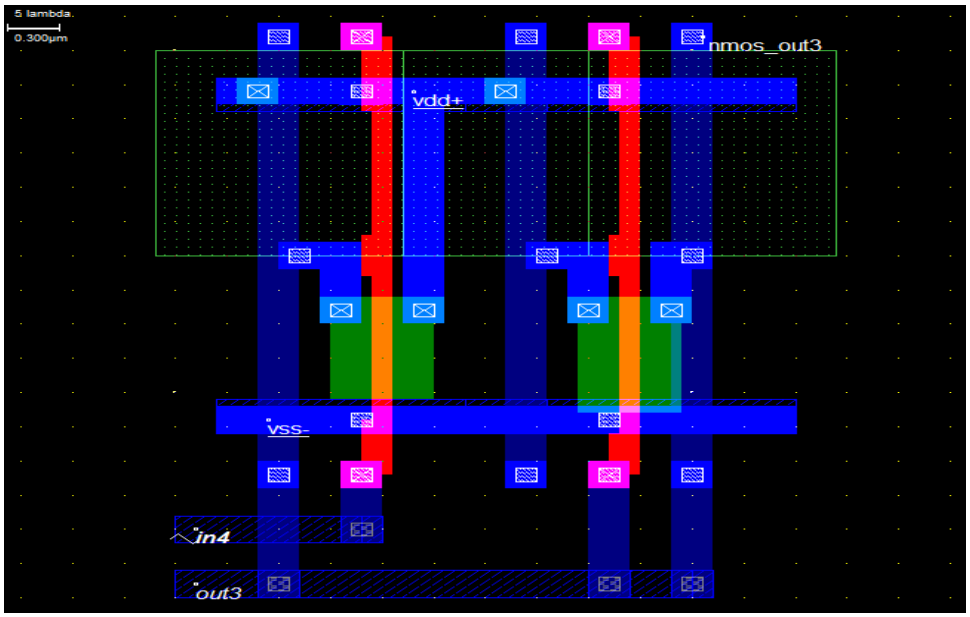
*microwind

THEORY:

A common-drain amplifier is one in which the input signal is applied to the gate and the output is taken from the source, making the drain common to both. Because it is common, there is no need for a drain resistor. A common-drain amplifier is shown below. A common-drain amplifier is also called a source-follower.

COMMON DRAIN AMPLIFIER:

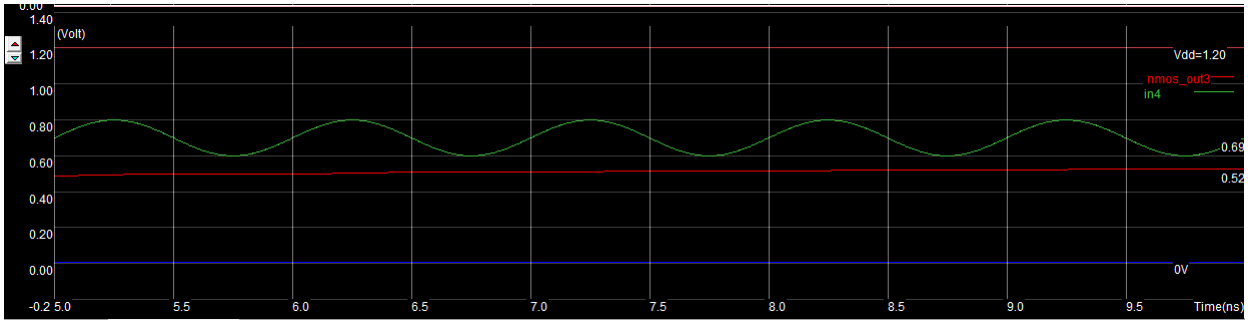


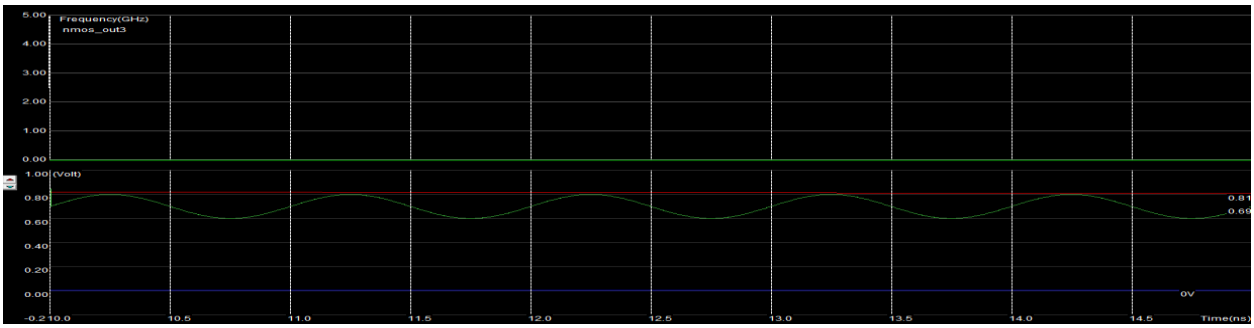

5 lambda
0.300µm
nmos_out3
vdd+
vss-
in4
out3

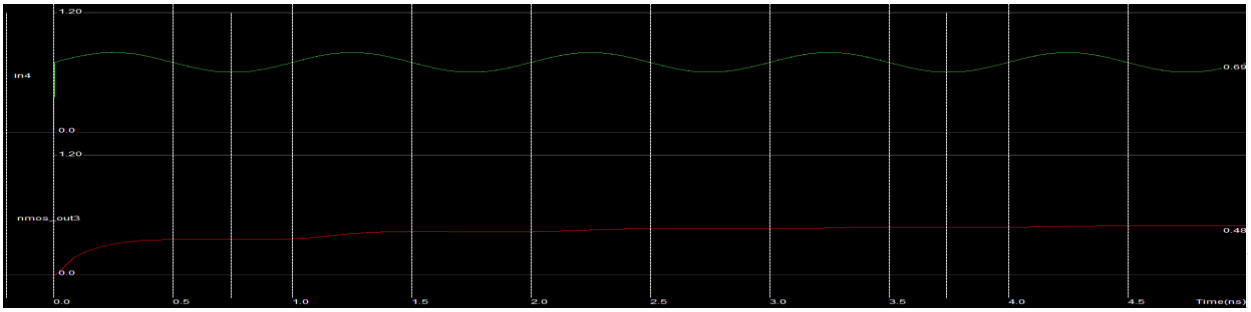
WAVE FORM

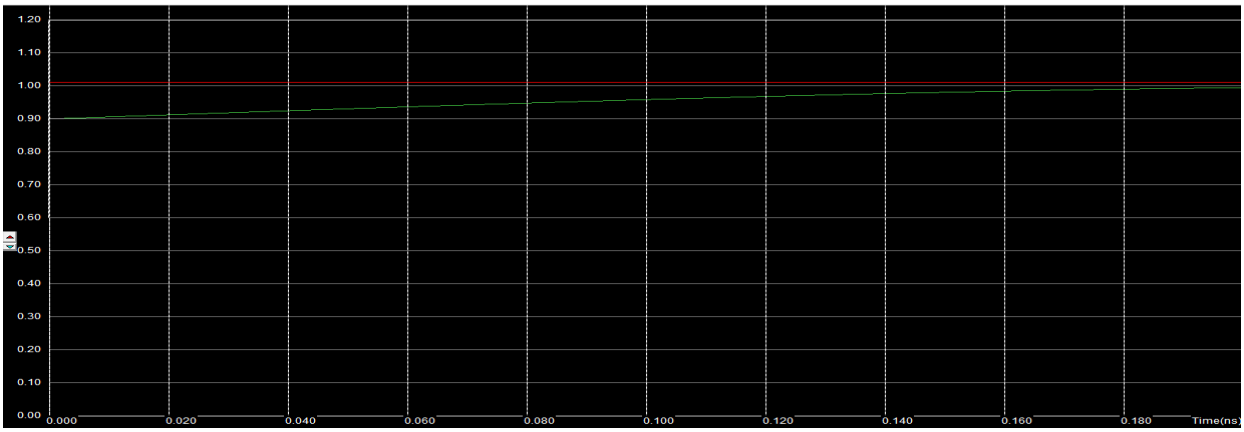
(NOTE:Double click in1=> click sinus

set =>AMP =0.1,OFFSET=0.7)









NET LIST:

```
CIRCUIT example
*
* IC Technology: CMOS 0.12µm - 6 Metal
*
VDD 1 0 DC 1.20
*
* List of nodes
* " nmos_out3" corresponds to n°3
* "N4" corresponds to n°4
* "in4" corresponds to n°5
*
* MOS devices
MN1 3 5 1 0 N1  W= 0.90U L= 0.12U
MN2 4 3 3 0 N1  W= 1.02U L= 0.12U
*
C2 1 0  2.578fF
C3 3 0  1.502fF
C4 4 0  0.497fF
C5 5 0  0.365fF
*
* n-MOS Model 3 :
* low leakage
.MODEL N1 NMOS LEVEL=3 VTO=0.40 UO=600.000 TOX= 2.0E-9
+LD =0.000U THETA=0.500 GAMMA=0.400
+PHI=0.200 KAPPA=0.060 VMAX=120.00K
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p CJSW=240.0p
*
* Transient analysis
*
.TEMP 27.0
.TRAN 0.1N 5.00N
* (Pspice)
.PROBE
.END
```

PROCEDURE:

1.Open microwind by double clicking on microwind.
2.Create new design by click on file-new
3.Select model file by click on file->select foundary and select the model file and save the file
4.Make Verilog file and click on generate
5.To run the simulation file
6.View the output waveform

PARTICULARS	MAXIMUM MARKS	MARKS OBTAINED
PREPARATION	30	
EXECUTION OF PRACTICAL	30	
CONCLUDING ACTIVITIES	30	
VIVA-VOCE	10	
TOTAL MARKS	100	

RESULT:

Thus the common drain schematic form was designed and simulated using microwind

EX.NO. 4 DESIGN AND SIMULATE COMMON

GATE GENERATE LAYOUT

AIM :

To design, synthesize, simulate and implement the CMOS gate in layout form using Microwind.

APPARATUS REQUIRED :

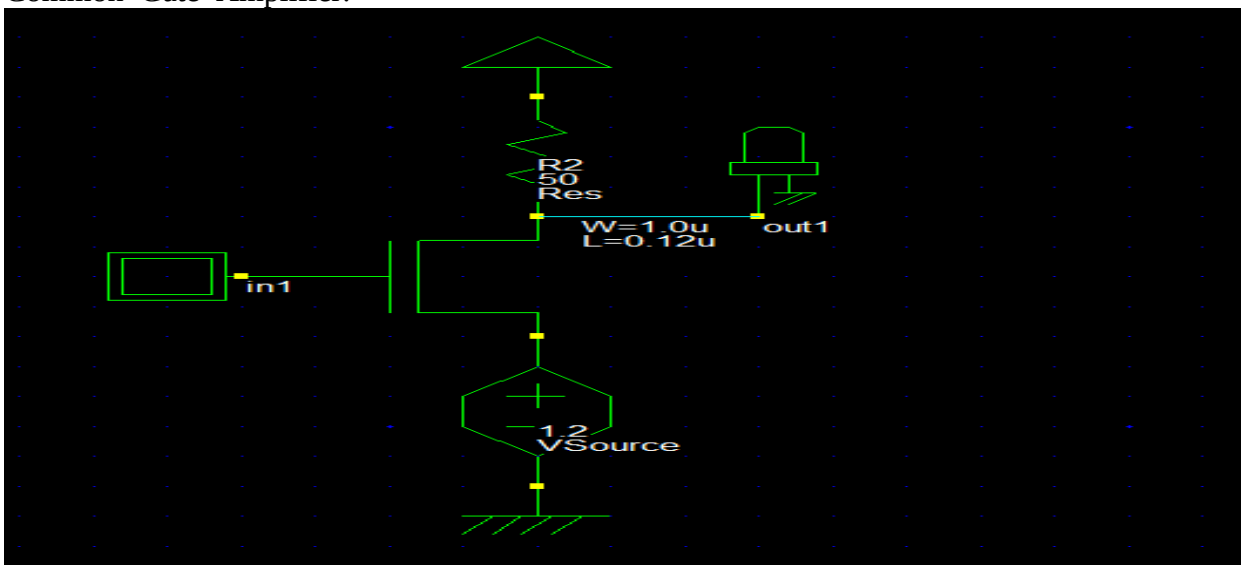
*PC

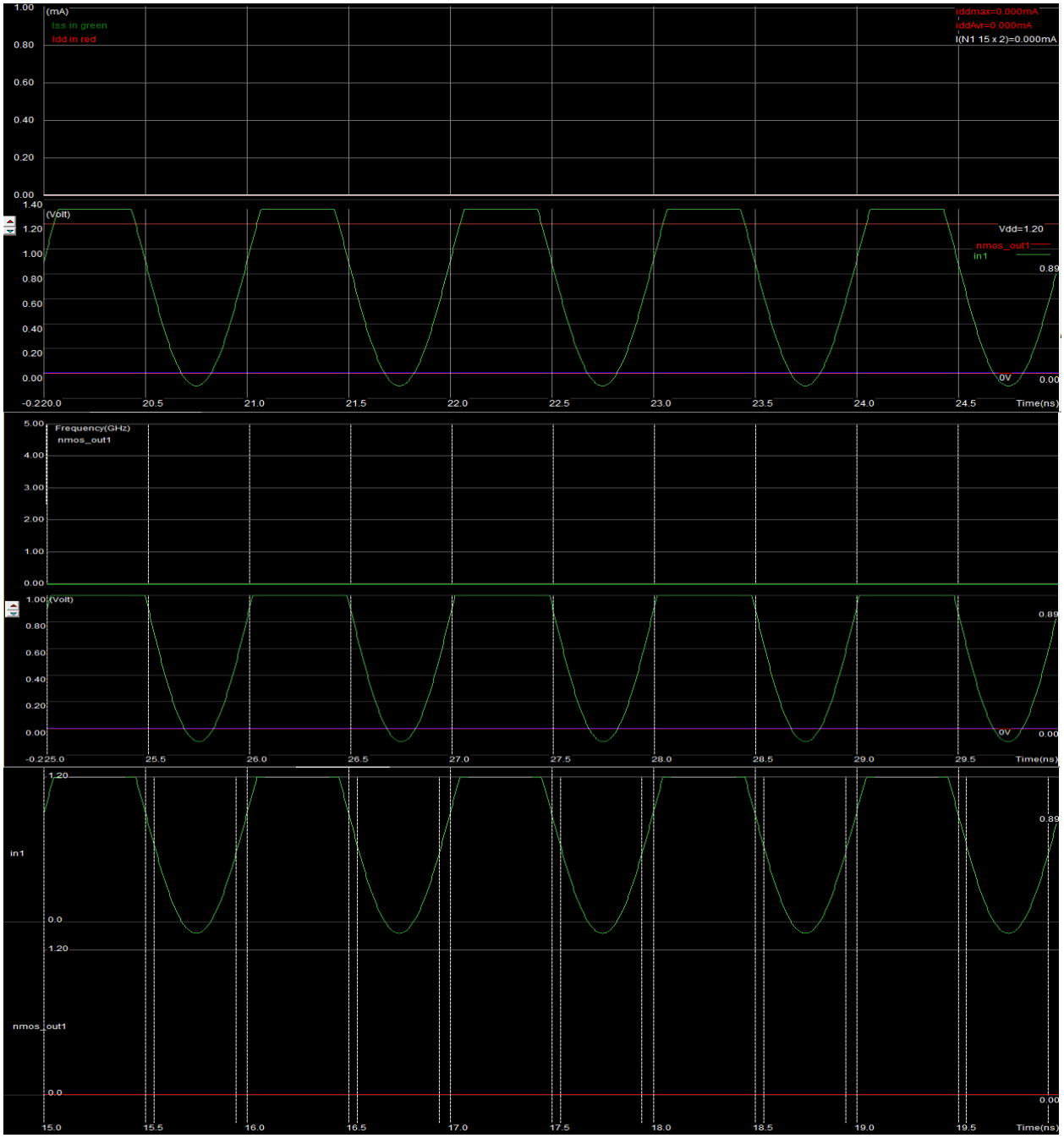
*microwind

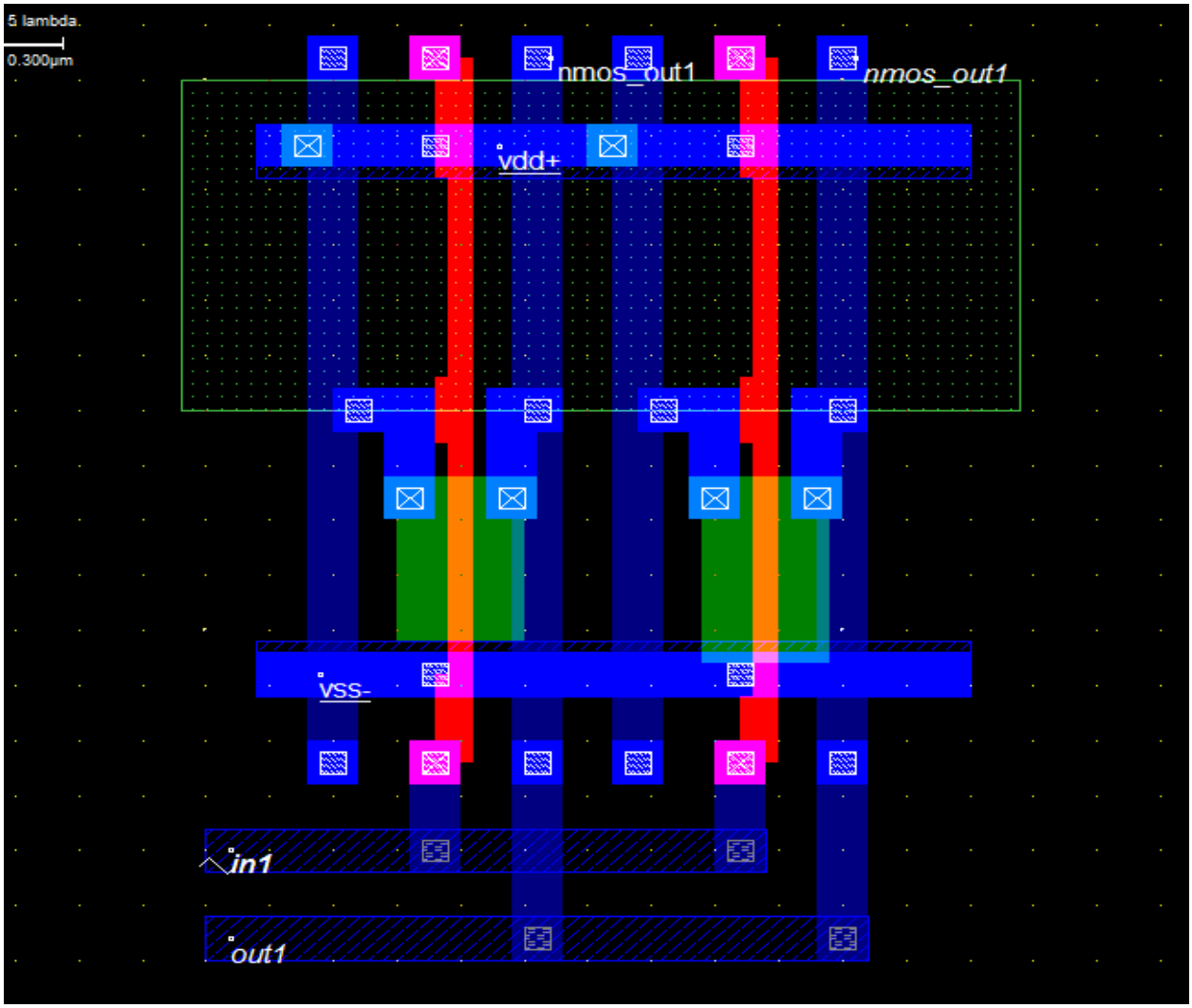
THEORY:

In common source amplifier and source follower circuits, the input signal is applied to the gate of a MOSFET. It is also possible to apply the input signal to the source terminal by keeping common gate terminal. This type of amplifier is called as common gate amplifier.

Common Gate Amplifier:




(mA)
Iss in green
Idd in red
Iddmax=0.000mA
IddAvr=0.000mA
I(N1 15 x 2)=0.000mA
(Volt)
Vdd=1.20
nmos_out1
in1
Time(ns)
Frequency(GHz)
nmos_out1
(Volt)
Time(ns)
in1
nmos_out1
Time(ns)


5 lambda
0.300µm
nmos_out1
nmos_out1
vdd+
vss-
in1
out1

NETLIST:

```
*
* IC Technology: CMOS 0.12µm - 6 Metal
*
VDD 1 0 DC 1.20
*
* List of nodes
* " nmos_out1" corresponds to n°3
* "N4" corresponds to n°4
* "N5" corresponds to n°5
* "in1" corresponds to n°6
*
* MOS devices
MN1 5 6 3 0 N1  W= 0.90U L= 0.12U
MN2 4 6 3 0 N1  W= 1.02U L= 0.12U
*
C2 1 0  2.262fF
C3 3 0  1.153fF
C4 4 0  0.497fF
C5 5 0  0.475fF
C6 6 0  0.737fF
*
* n-MOS Model 3 :
* low leakage
.MODEL N1 NMOS LEVEL=3 VTO=0.40 UO=600.000 TOX= 2.0E-9
+LD =0.000U THETA=0.500 GAMMA=0.400
+PHI=0.200 KAPPA=0.060 VMAX=120.00K
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p CJSW=240.0p
*
* Transient analysis
*
.TEMP 27.0
.TRAN 0.1N 5.00N
* (Pspice)
.PROBE
.END
```

PROCEDURE:

1.Open microwind by double clicking on microwind.
2.Create new design by click on file-new
3.Select model file by click on file->select foundary and select the model file and save the file
4.Make Verilog file and click on generate
5.To run the simulation file
6.View the output waveform

PARTICULARS	MAXIMUM MARKS	MARKS OBTAINED
PREPARATION	30	
EXECUTION OF PRACTICAL	30	
CONCLUDING ACTIVITIES	30	
VIVA-VOCE	10	
TOTAL MARKS	100	

RESULT:

Thus the common gate schematic form was designed and simulated using microwind

EX.NO. 5 Design a differential amplifier with resistive load using transistors

AIM :

To design, synthesize, simulate and implement the differential amplifier with resistive load using transistors in layout form using Microwind.

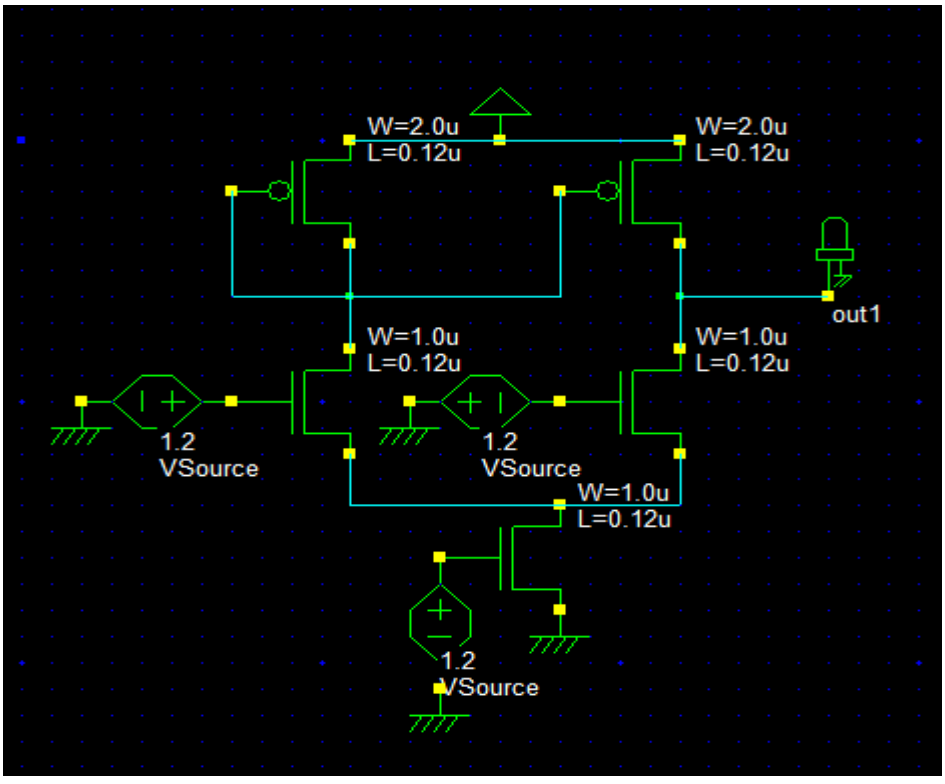
APPARATUS REQUIRED :

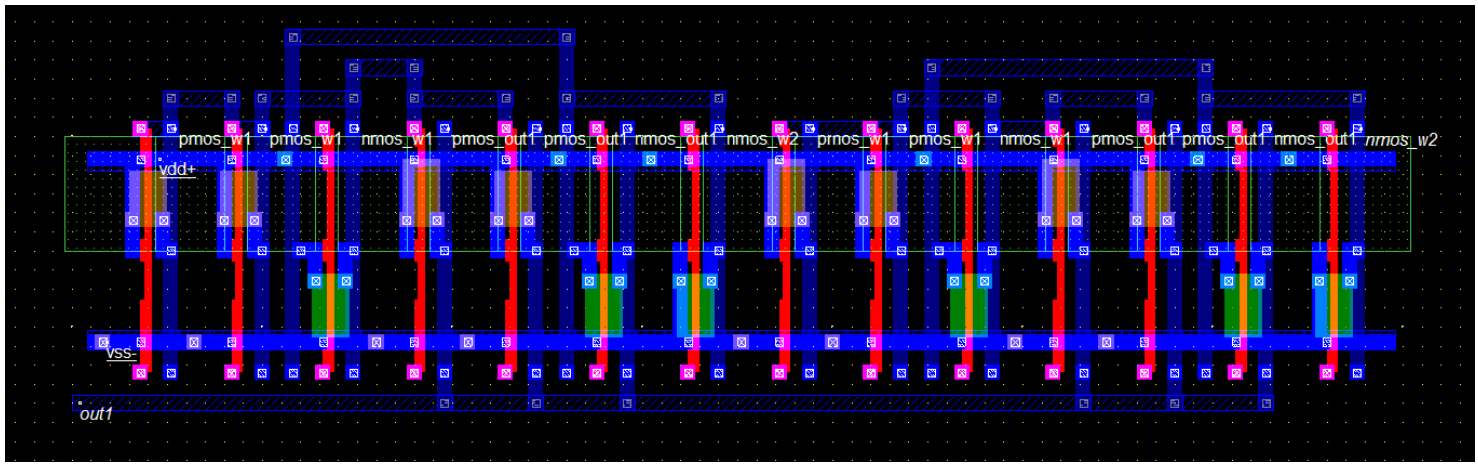
*PC

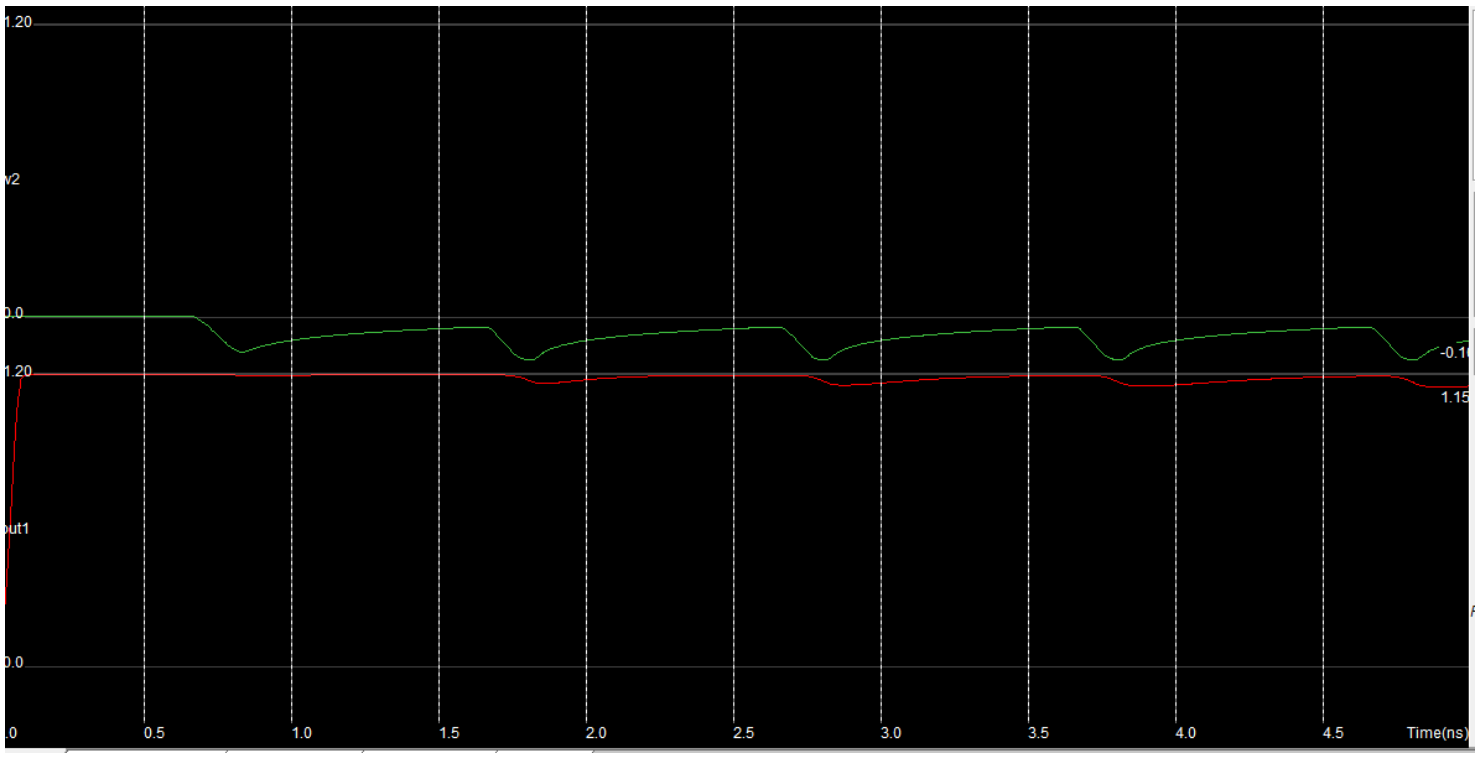
*microwind

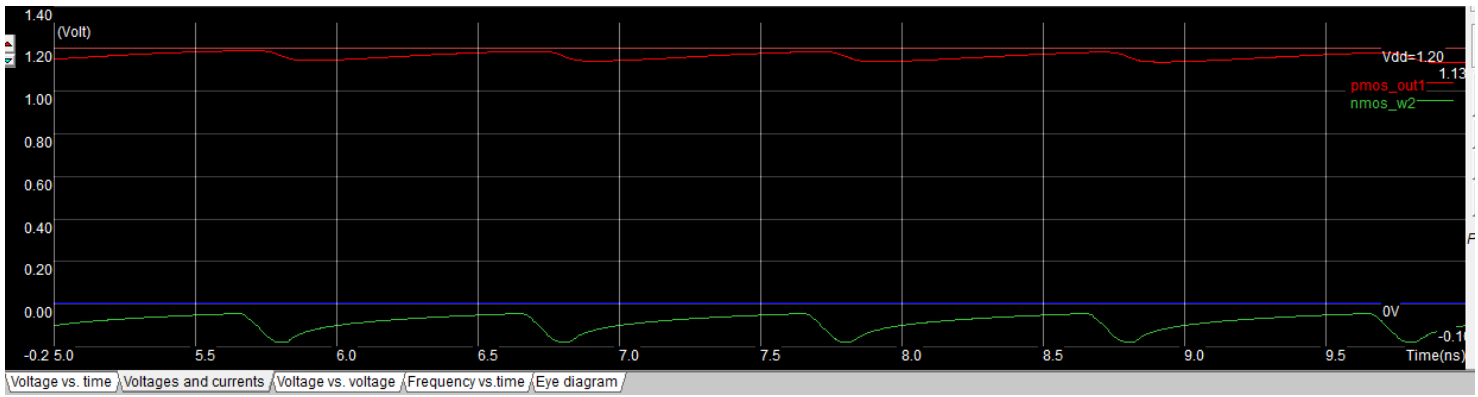
THEORY: Differential amplifiers are used as a means of suppressing common-mode noise. In this way, common-mode noise superimposed on the op amp input stage is eliminated. However, if noise is superimposed on the GND or power supply of the op amp, this noise will be superimposed on the output.

DIFFERENTIAL AMPLIFIER:




pmos_w1
pmos_w1
nmos_w1
pmos_out1
pmos_out1
nmos_out1
nmos_w2
pmos_w1
pmos_w1
nmos_w1
pmos_out1
pmos_out1
nmos_out1
nmos_w2
vdd+
vss-
out1


1.20
v2
0.0
1.20
ut1
0.0
-0.1
1.15
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
Time(ns)


1.40
(Volt)
1.20
1.00
0.80
0.60
0.40
0.20
0.00
-0.2
5.0
5.5
6.0
6.5
7.0
7.5
8.0
8.5
9.0
9.5
Time(ns)
Vdd=1.20
1.13
pmos_out1
nmos_w2
0V
-0.1
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram

NETLIST

```
CIRCUIT Z:\mw-tools\Export dsch2\diff_amp.sch
*
* IC Technology: CMOS 0.12µm - 6 Metal
*
VDD 1 0 DC 1.20
*
* List of nodes
* " pmos_out1" corresponds to n°3
* " nmos_w1" corresponds to n°5
* " nmos_w2" corresponds to n°6
* "N7" corresponds to n°7
* "N8" corresponds to n°8
* "N9" corresponds to n°9
*
* MOS devices
MN1 0 7 6 0 N1  W= 1.02U L= 0.12U
MN2 6 8 3 0 N1  W= 1.02U L= 0.12U
MN3 6 9 5 0 N1  W= 1.02U L= 0.12U
MP1 1 5 3 1 P1  W= 1.98U L= 0.12U
MP2 1 5 5 1 P1  W= 1.80U L= 0.12U
*
C2 1 0  7.473fF
C3 3 0  1.826fF
C5 5 0  3.071fF
C6 6 0  1.903fF
C7 7 0  0.296fF
C8 8 0  0.296fF
C9 9 0  0.296fF
*
* n-MOS Model 3 :
* low leakage
.MODEL N1 NMOS LEVEL=3 VTO=0.40 UO=600.000 TOX= 2.0E-9
+LD =0.000U THETA=0.500 GAMMA=0.400
+PHI=0.200 KAPPA=0.060 VMAX=120.00K
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p CJSW=240.0p
*
* p-MOS Model 3:
* low leakage
.MODEL P1 PMOS LEVEL=3 VTO=-0.45 UO=200.000 TOX= 2.0E-9
+LD =0.000U THETA=0.300 GAMMA=0.400
+PHI=0.200 KAPPA=0.060 VMAX=110.00K
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p CJSW=240.0p
*
* Transient analysis
*
.TEMP 27.0
.TRAN 0.1N 5.00N
* (Pspice)
.PROBE
.END
```

PROCEDURE:

1.Open microwind by double clicking on microwind.
2.Create new design by click on file-new
3.Select model file by click on file->select foundary and select the model file and save the file
4.Make Verilog file and click on generate
5.To run the simulation file
6.View the output waveform

PARTICULARS	MAXIMUM MARKS	MARKS OBTAINED
PREPARATION	30	
EXECUTION OF PRACTICAL	30	
CONCLUDING ACTIVITIES	30	
VIVA-VOCE	10	
TOTAL MARKS	100	

RESULT:

Thus the differential amplifier with resisitive load schematic form was designed and simulated using microwind

EX.NO. 6 Design three stage and five stage ring oscillator circuit and compare its frequencies.

AIM :

To design, synthesize, simulate and implement the three stage and five stage ring oscillator circuit and compare its frequencies **.**

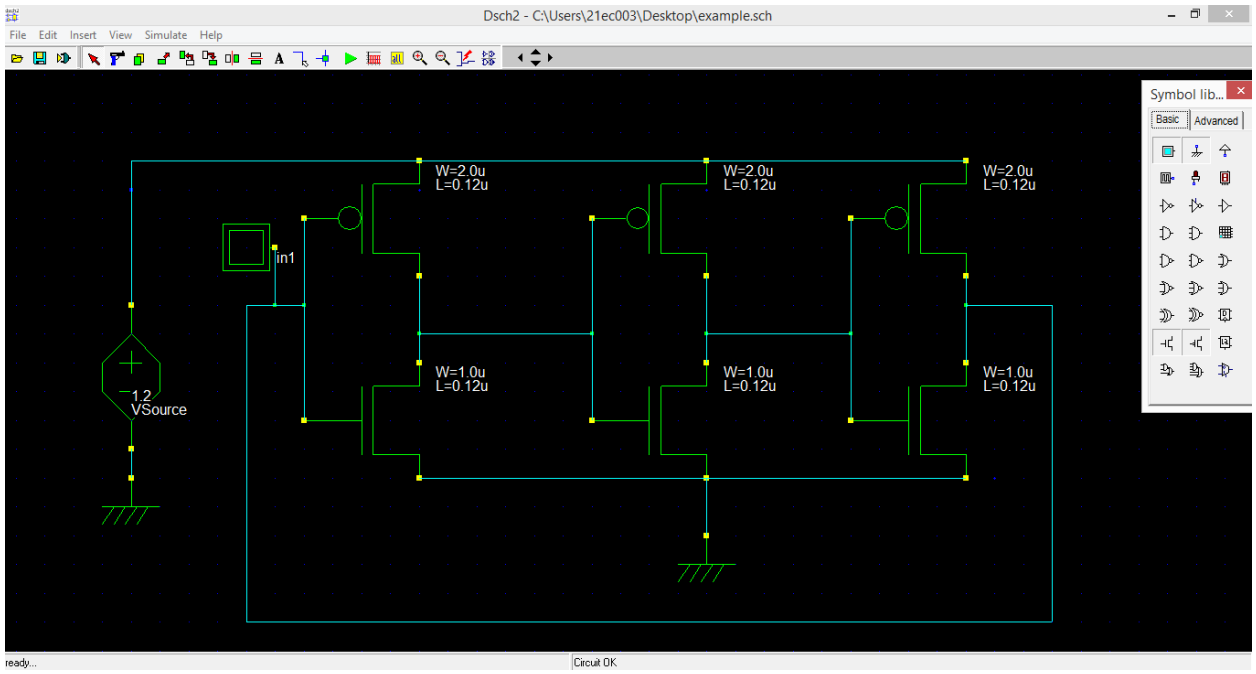
APPARATUS REQUIRED :

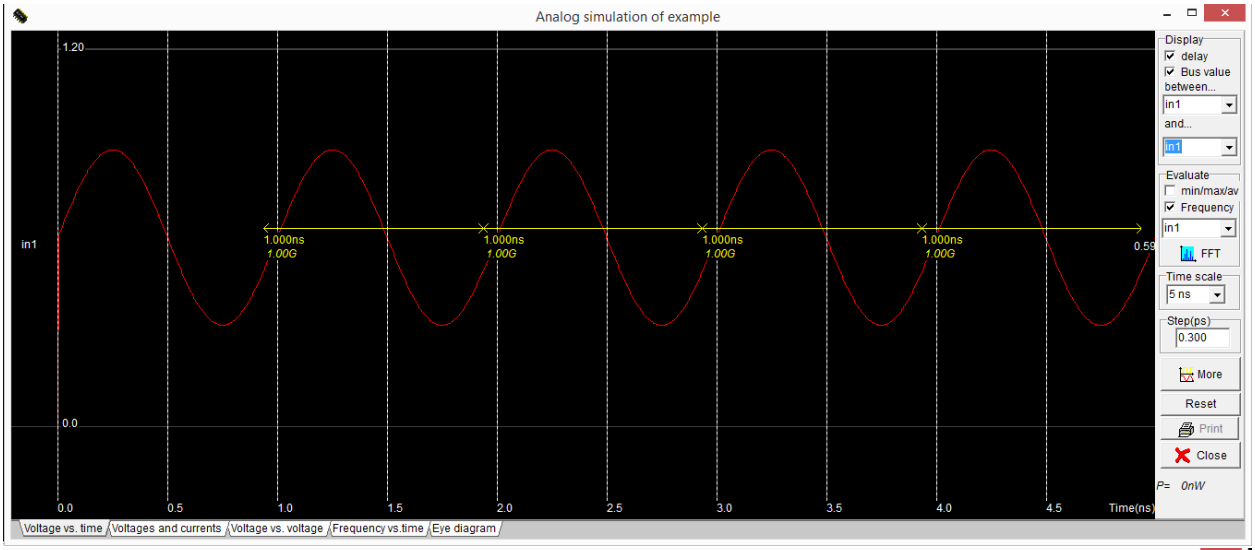
*PC

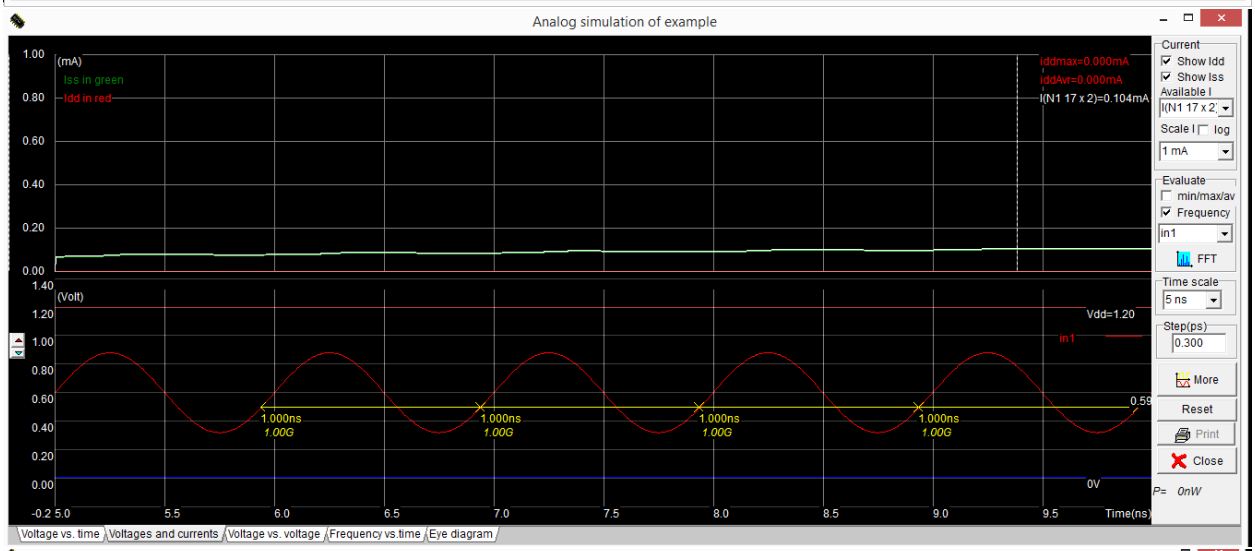
*microwind

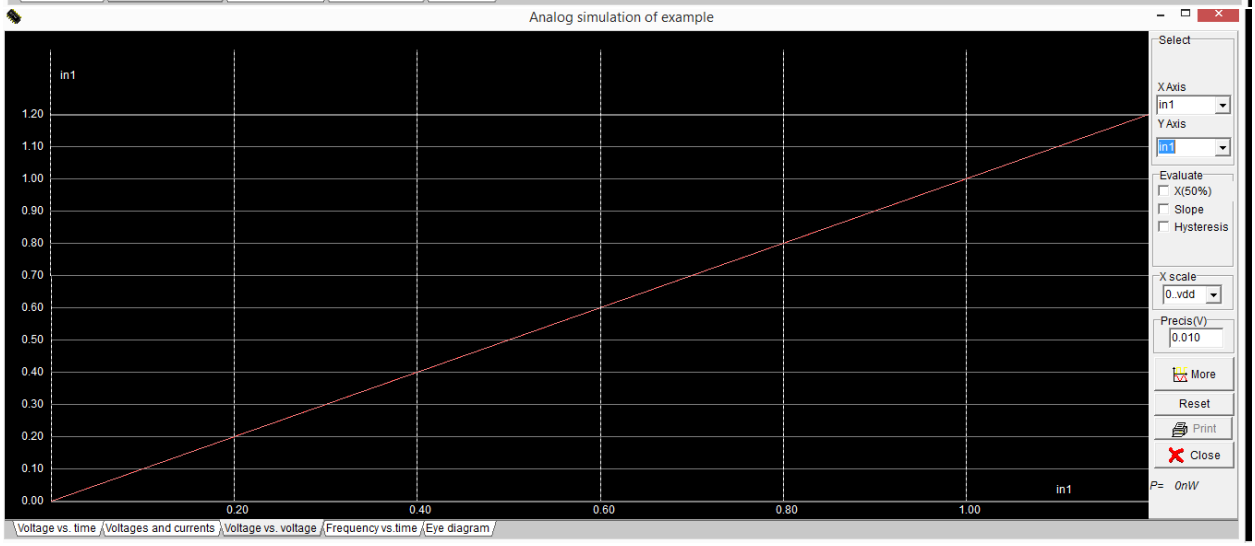
THEORY: The ring oscillator is "an odd number of inverters are connected in a series form with positive feedback & output oscillates between two voltage levels either 1 or zero to measure the speed of the process. In place of inverters, we can define it with NOT gates also. These oscillators have an 'n' odd number of inverters. For instance, if this oscillator has 3 inverters then it is called a three-stage ring oscillator. If the inverter count is seven then it is seven stage ring oscillator. The number of inverter stages in this oscillator mainly depends on the frequency which we want to generate from this oscillator.

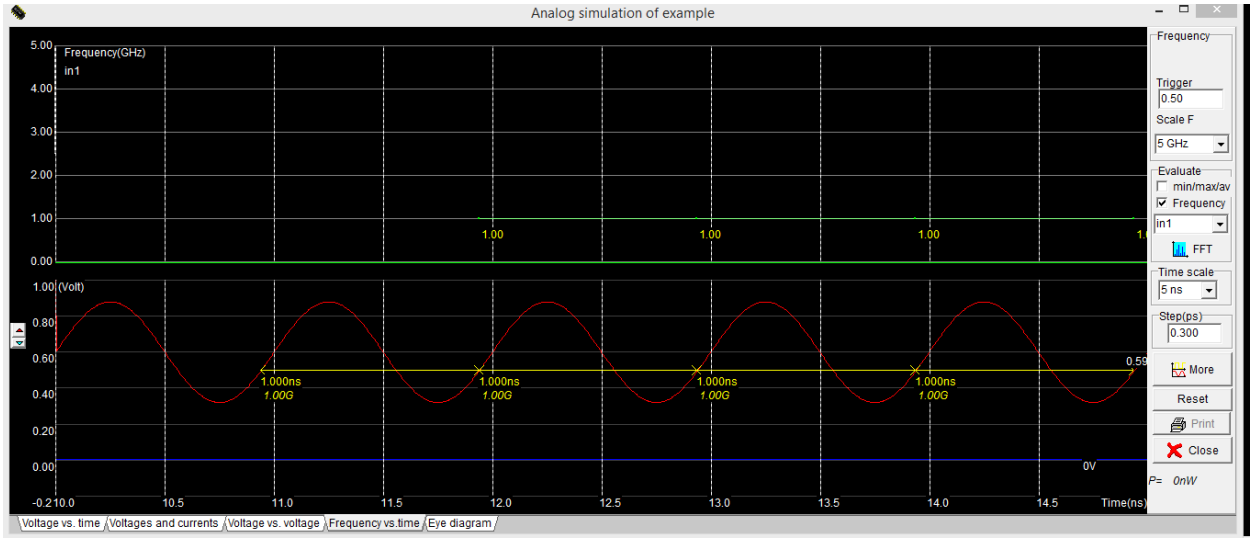
3 STAGE RING OSCILLATOR:



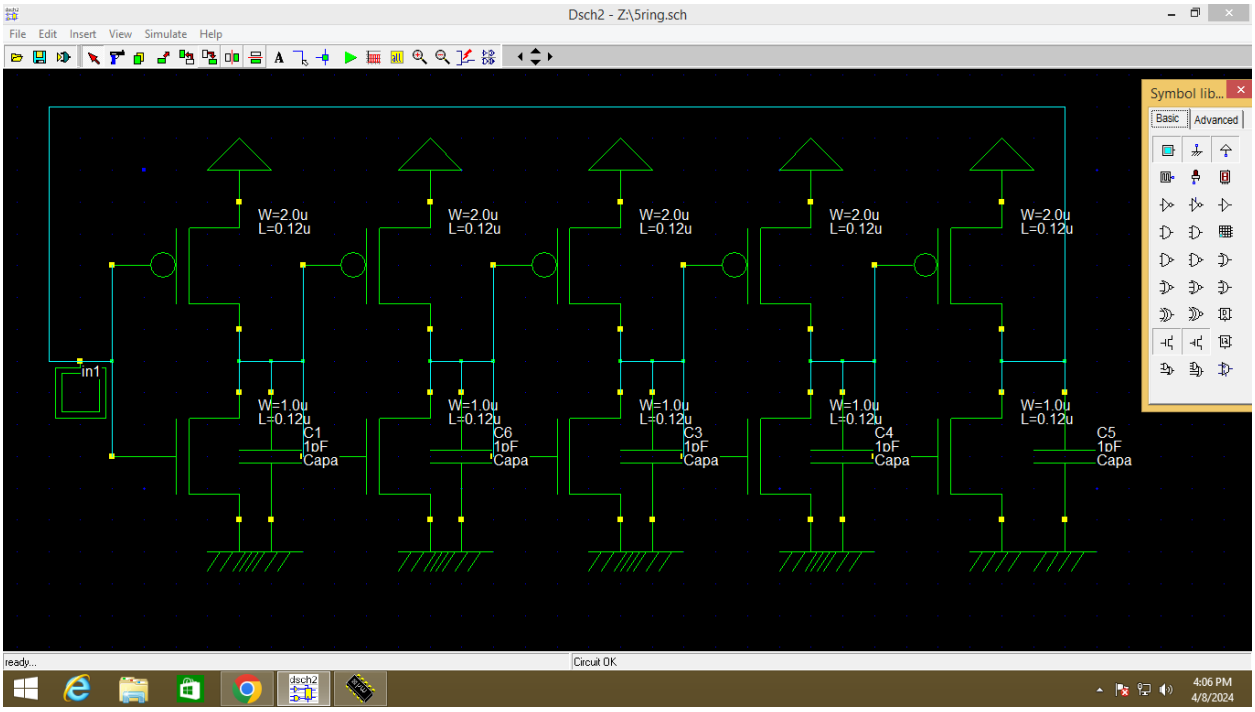

Analog simulation of example
1.20
0.0
in1
1.000ns
1.00G
0.59
Time(ns)
Display
delay
Bus value
between...
and...
Evaluate
min/max/av
Frequency
FFT
Time scale
5 ns
Step(ps)
0.300
More
Reset
Print
Close
P= 0nW
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram

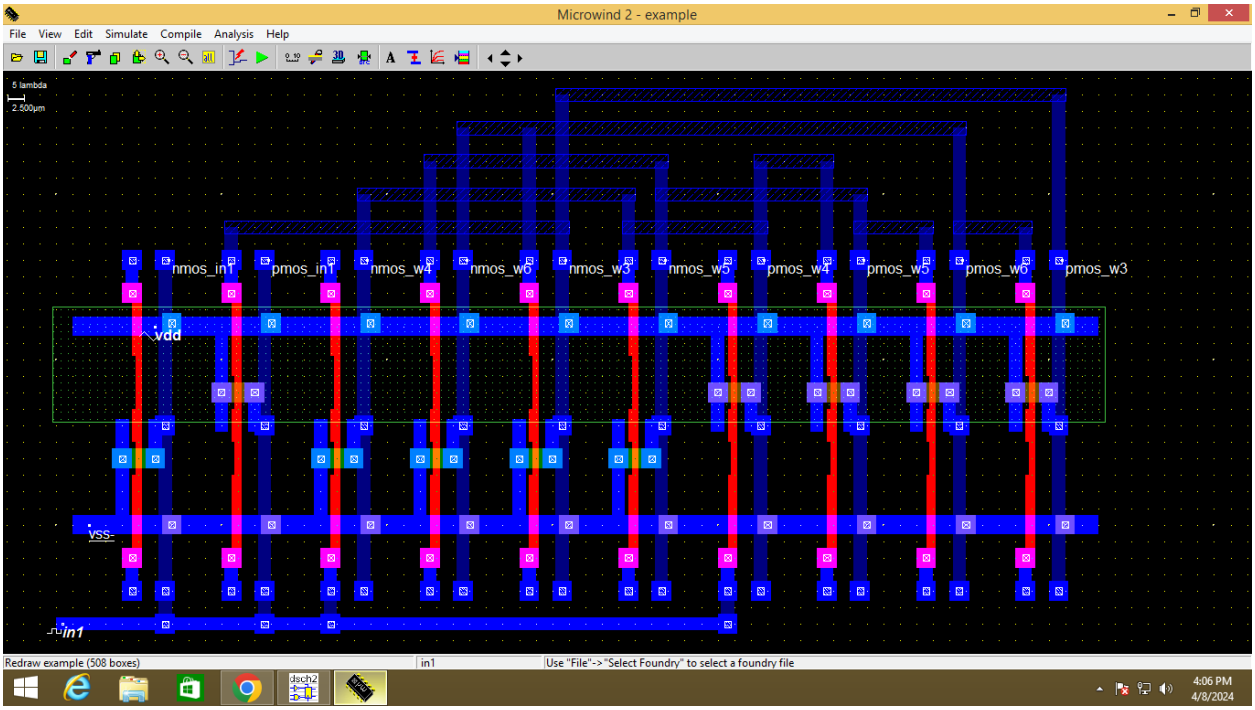

Analog simulation of example
(mA)
Iss in green
Idd in red
iddmax=0.000mA
iddAvr=0.000mA
I(N1 17 x 2)=0.104mA
(Volt)
Vdd=1.20
in1
0V
1.000ns
1.00G
0.59
Time(ns)
Current
Show Idd
Show Iss
Available I
Scale I
log
1 mA
Evaluate
min/max/av
Frequency
FFT
Time scale
5 ns
Step(ps)
0.300
More
Reset
Print
Close
P= 0nW
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram

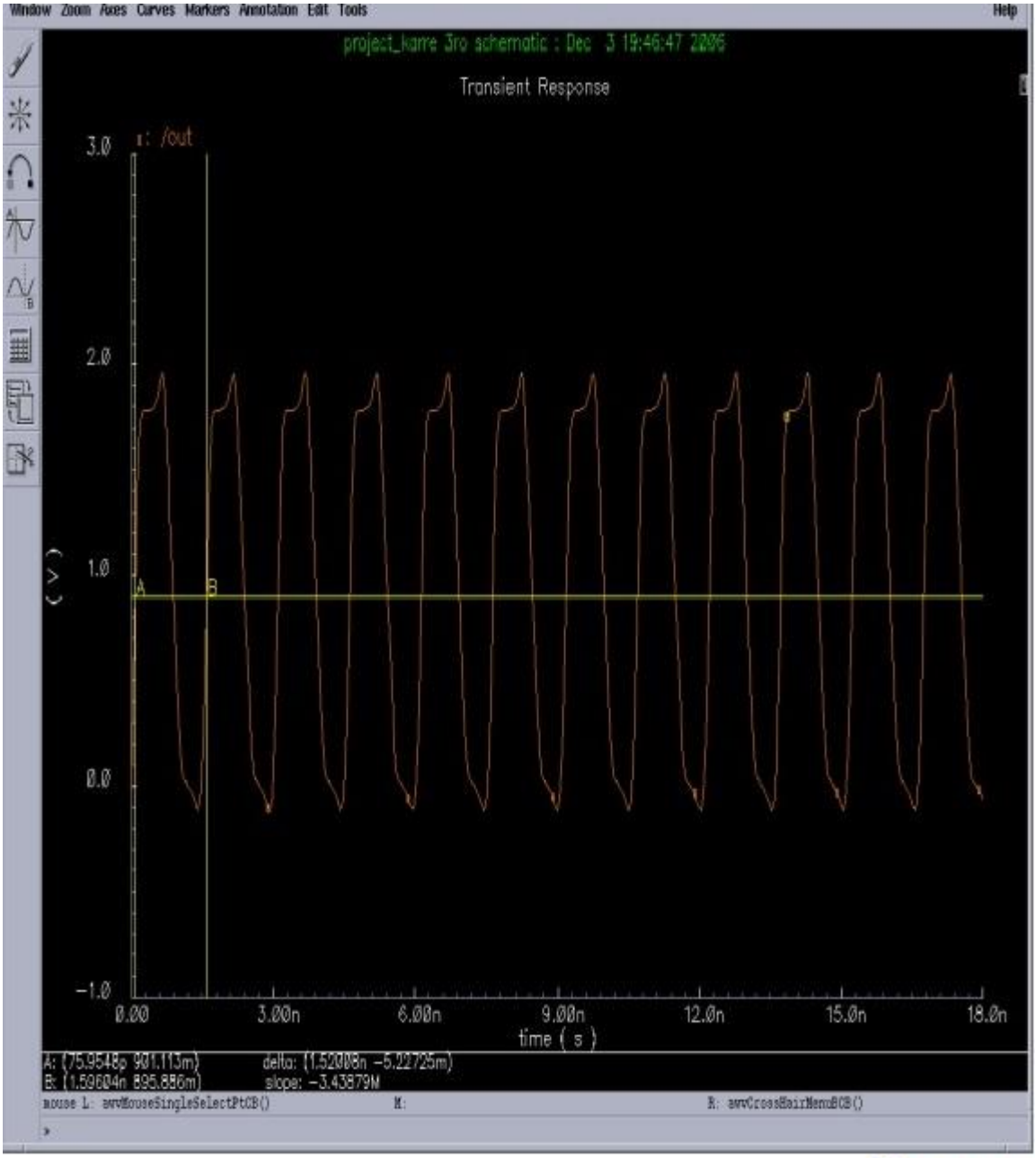

Analog simulation of example
in1
Select
X Axis
in1
Y Axis
in1
Evaluate
X(50%)
Slope
Hysteresis
X scale
0..vdd
Precis(V)
0.010
More
Reset
Print
Close
P= 0nW
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram



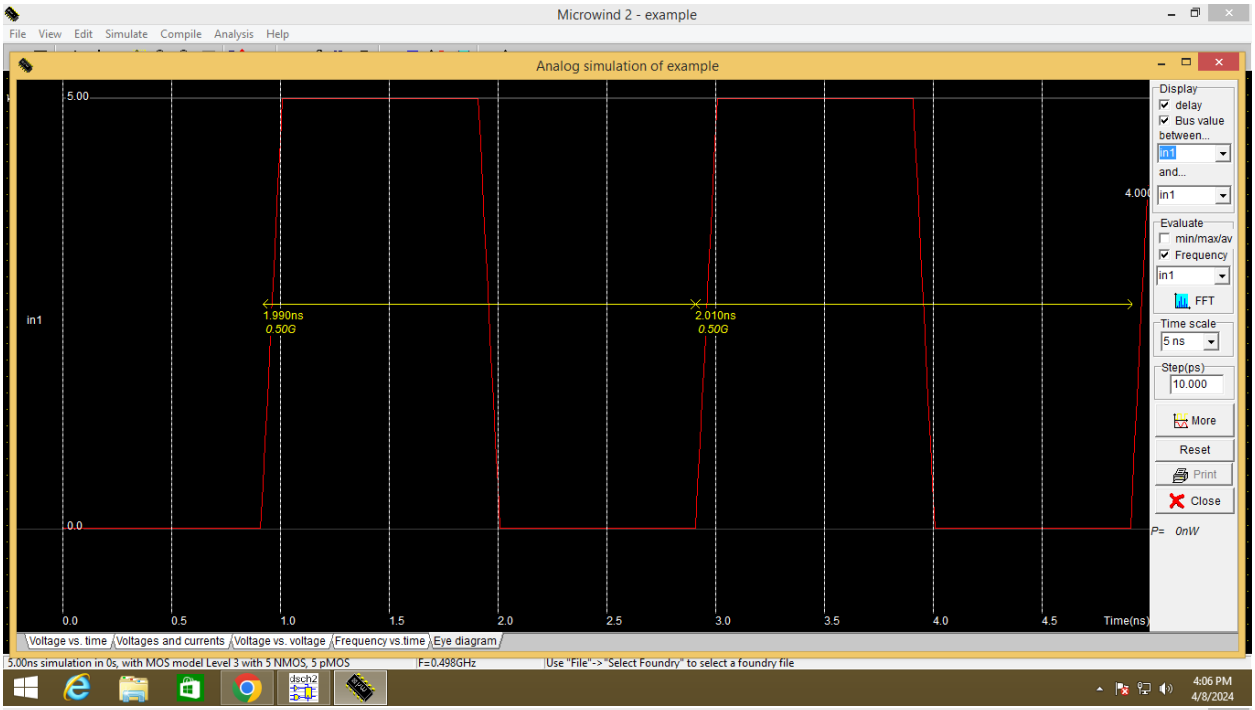
5 STAGE RING OSCILLATOR:

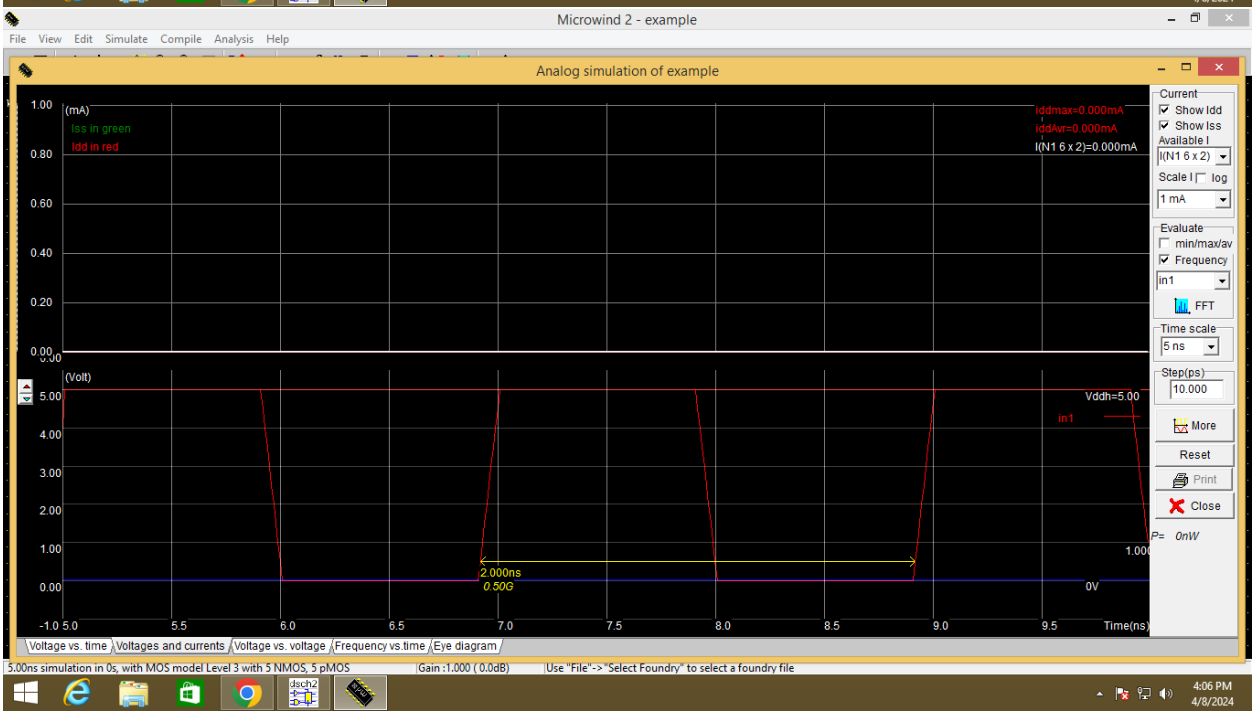


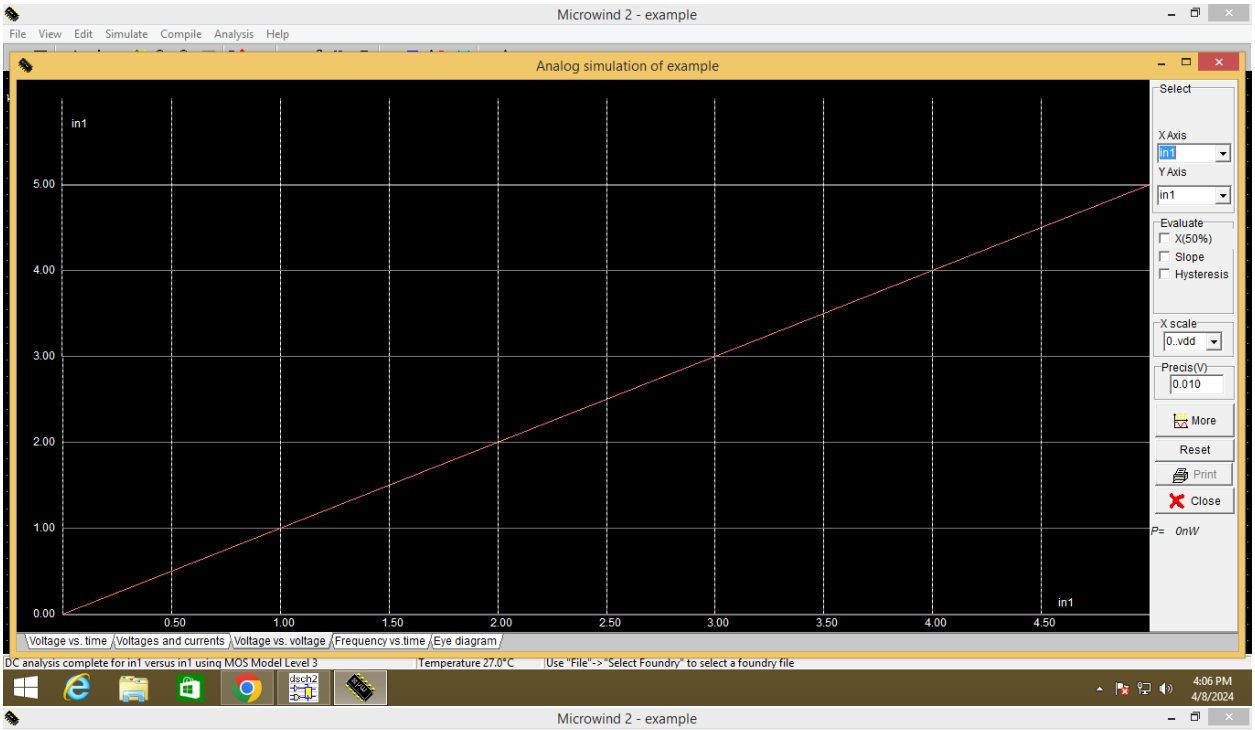

Microwind 2 - example
File View Edit Simulate Compile Analysis Help
5 lambda
2.500µm
nmos_in1
pmos_in1
nmos_w4
nmos_w6
nmos_w3
nmos_w5
pmos_w4
pmos_w5
pmos_w6
pmos_w3
vdd
vss
in1
Redraw example (508 boxes)
in1
Use "File"-> "Select Foundry" to select a foundry file
4:06 PM
4/8/2024

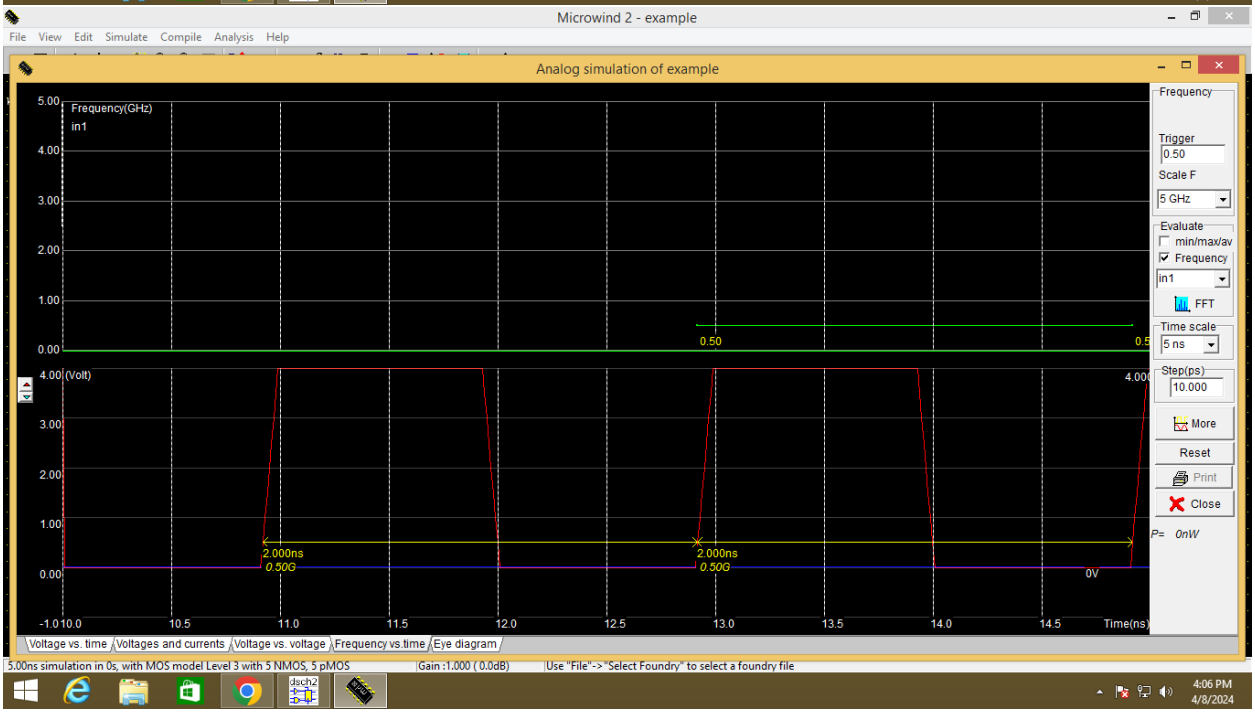


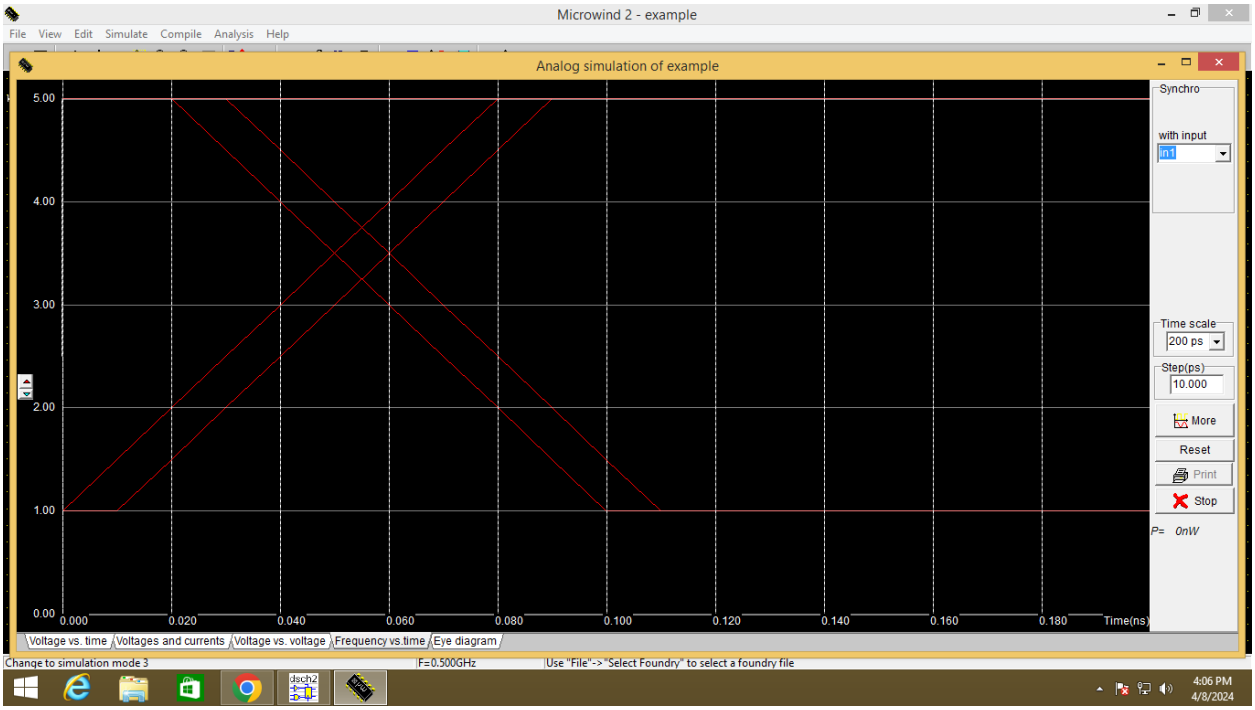
Elprocus.com


Microwind 2 - example
File View Edit Simulate Compile Analysis Help
Analog simulation of example
5.00
0.0
in1
1.990ns
0.50G
2.010ns
0.50G
4.00
0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5 Time(ns)
Display
delay
Bus value between...
in1
and...
in1
Evaluate
min/max/av
Frequency
in1
FFT
Time scale
5 ns
Step(ps)
10.000
More
Reset
Print
Close
P= 0nW
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram
5.00ns simulation in 0s, with MOS model Level 3 with 5 NMOS, 5 pMOS
F=0.498GHz
Use "File"-> "Select Foundry" to select a foundry file
4:06 PM
4/8/2024


Microwind 2 - example
File View Edit Simulate Compile Analysis Help
Analog simulation of example
1.00
(mA)
Iss in green
Idd in red
0.80
0.60
0.40
0.20
0.00
iddmax=0.000mA
iddAvr=0.000mA
I(N1 6 x 2)=0.000mA
(Volt)
5.00
4.00
3.00
2.00
1.00
0.00
-1.0 5.0 5.5 6.0 6.5 7.0 7.5 8.0 8.5 9.0 9.5 Time(ns)
Vddh=5.00
in1
2.000ns
0.50G
1.00
0V
Current
Show Idd
Show Iss
Available I
I(N1 6 x 2)
Scale I log
1 mA
Evaluate
min/max/av
Frequency
in1
FFT
Time scale
5 ns
Step(ps)
10.000
More
Reset
Print
Close
P= 0nW
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram
5.00ns simulation in 0s, with MOS model Level 3 with 5 NMOS, 5 pMOS
Gain :1.000 (0.0dB)
Use "File"-> "Select Foundry" to select a foundry file
4:06 PM
4/8/2024


Microwind 2 - example
File View Edit Simulate Compile Analysis Help
Analog simulation of example
in1
5.00
4.00
3.00
2.00
1.00
0.00
0.50
1.00
1.50
2.00
2.50
3.00
3.50
4.00
4.50
in1
Select
X Axis
in1
Y Axis
in1
Evaluate
X(50%)
Slope
Hysteresis
X scale
0..vdd
Precis(V)
0.010
More
Reset
Print
Close
P= 0nW
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram
DC analysis complete for in1 versus in1 using MOS Model Level 3
Temperature 27.0°C
Use "File"-> "Select Foundry" to select a foundry file
4:06 PM
4/8/2024


Microwind 2 - example
File View Edit Simulate Compile Analysis Help
Analog simulation of example
Frequency(GHz)
in1
5.00
4.00
3.00
2.00
1.00
0.00
0.50
4.00 (Volt)
3.00
2.00
1.00
0.00
2.000ns
0.50G
2.000ns
0.50G
0V
-1.0 10.0
10.5
11.0
11.5
12.0
12.5
13.0
13.5
14.0
14.5
Time(ns)
Frequency
Trigger
0.50
Scale F
5 GHz
Evaluate
min/max/av
Frequency
in1
FFT
Time scale
5 ns
Step(ps)
10.000
More
Reset
Print
Close
P= 0nW
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram
5.00ns simulation in 0s, with MOS model Level 3 with 5 NMOS, 5 pMOS
Gain :1.000 (0.0dB)
Use "File"-> "Select Foundry" to select a foundry file
4:06 PM
4/8/2024


Microwind 2 - example
File View Edit Simulate Compile Analysis Help
Analog simulation of example
5.00
4.00
3.00
2.00
1.00
0.00
0.000 0.020 0.040 0.060 0.080 0.100 0.120 0.140 0.160 0.180
Time(ns)
Synchro
with input
in1
Time scale
200 ps
Step(ps)
10.000
More
Reset
Print
Stop
P= 0nW
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram
Change to simulation mode 3
F=0.500GHz
Use "File"-> "Select Foundry" to select a foundry file
4:06 PM
4/8/2024

Calcualation:

The frequency of oscillation formula for this oscillator is
F=1/2nT
Here T=time delay for single inverter
N=number of inverters in the oscillator.

3 stage ring oscillator frequency:
F=1/2*3*2=0.08 HZ

5 stage ring oscillator frequency:
F=1/2*5*3=0.033HZ

PROCEDURE:

1.Open microwind by double clicking on microwind.
2.Create new design by click on file-new
3.Select model file by click on file->select foundary and select the model file and save the file
4.Make Verilog file and click on generate
5.To run the simulation file
6.View the output waveform

PARTICULARS	MAXIMUM MARKS	MARKS OBTAINED
PREPARATION	30	
EXECUTION OF PRACTICAL	30	
CONCLUDING ACTIVITIES	30	
VIVA-VOCE	10	
TOTAL MARKS	100	

RESULT:

Thus the three stage and five stage ring oscillator circuit and compare its frequencies.schematic form was designed and simulated usingmicrowind